CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A simultaneous bi-directional data bus comprising:

a simultaneous bi-directional data bus having a characteristic impedance Z0;

a first driver unit and receiver unit connected to a first terminal end of the simultaneous bi-directional data bus;

a second driver unit and receiver unit connected to a second terminal end of the simultaneous bi-directional data bus;

each of the first driver unit and the second driver unit having a sourcing current source and a first resistor connected in parallel between a voltage supply and a terminal end of the simultaneous bi-directional data bus, and a sinking current source and a second resistor connected in parallel between a ground and a terminal end of the simultaneous bi-directional data bus, wherein a substantially higher impedance of each current source relative to a substantially lower impedance of each resistor connected in parallel to the current source provides a relatively constant impedance in each driver unit which substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

2. The simultaneous bi-directional data bus of claim 1 where, in each of the first driver unit and the second driver unit, the first resistor of the sourcing current source and the second resistor of the sinking current source is substantially equal to twice the characteristic impedance of the simultaneous bi-directional data bus.

3. The simultaneous bi-directional data bus of claim 1, wherein the sourcing current sources of each of the first driver unit and the second driver unit are identical sourcing

current sources, and the sinking current sources of each of the first driver unit and the second driver unit are identical sinking current sources.

4. The simultaneous bi-directional data bus of claim 1, wherein each driver unit comprises a p side driver and an n side driver which are serially connected between a voltage supply and ground, with the connection between the serially connected drivers being connected to the simultaneous bi-directional data bus, and each driver unit has an output impedance of substantially twice the characteristic impedance of the simultaneous bi-directional data bus so that the total output impedance of each driver unit substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

5. The simultaneous bi-directional data bus of claim 1, wherein each driver unit includes a set of programmable compensation capacitors to compensate for parasitic capacitance and to accelerate transitions to higher speeds.

6. The simultaneous bi-directional data bus of claim 1, wherein each sinking current source includes a pfet device, with its gate coupled to an input, coupled to the power supply, with the pfet device being coupled through first, second and third resistors to ground, with a plurality of programmable pfet devices and series connected compensating capacitors being connected in parallel with the second resistor, and the connection between the first and second resistors being connected to the gate of an nfet device.

7. The simultaneous bi-directional data bus of claim 1, wherein each sinking current source includes a pfet device P0s, with its gate coupled to an input Vin, coupled to the power supply Vcc, with the pfet device being coupled through first, second and third resistors Rgn1, Rgn2 and Rgn3 to ground 0V, with a plurality of programmable pfet devices P1, P2, Pk and series connected compensating capacitors Cn1, Cn2, Cnk being connected in parallel with the second resistor Rgn2, and the connection between the first

and second resistors Rgn1, Rgn2 being connected to the gate of an nfet device N0, and the gate-source voltage of the nfet device N0 $Vgn = Vcc*Rgn2/(Rgn1+Rgn2+Rgn3)$ when Vin is at logic 0 and P0s is turned on.

8. The simultaneous bi-directional data bus of claim 7, wherein each current source provides the same amount of current I0, and the nfet device N0 and the values of Rgn1, Rgn2 and Rgn3 are chosen to meet the following requirements:
the drain to source current Ids of N0 is I0 when $Vgn1 = Vcc*Rgn1/(Rgn1+Rgn2+Rgn3)$, and Vgn1 − Vthn, the threshold voltage of N0, $< (Vcc-I0*Z0)/2$, so that N0 is at a saturation region/mode when turned on.

9. The simultaneous bi-directional data bus of claim 8, wherein when a logic low is applied to one or more of the gates of P1, P2 ...Pk, the corresponding capacitors are selected, and when Vin is transiting from a logic high to a logic low, the resistor Rgn2 is shorted by the compensation capacitors.

10. The simultaneous bi-directional data bus of claim 1, wherein each sourcing current source includes an nfet device, having its gate coupled to an input, coupled to ground, with the nfet device being coupled through first, second and third resistors to the power supply, with a plurality of programmable nfet devices and series connected compensating capacitors being connected in parallel with the second resistor, and the connection between the first and second resistors being connected to the gate of a pfet device.

11. The simultaneous bi-directional data bus of claim 1, wherein each sourcing current source includes an nfet device N0s, having its gate coupled to an input Vin, coupled to ground 0V, with the nfet device being coupled through first, second and third resistors Rgp1, Rgp2, Rgp3 to the power supply Vcc, with a plurality of programmable nfet devices N1, N2, Nk and series connected compensating capacitors Cp1, Cp2, Cpk being

connected in parallel with the second resistor Rgp2, and the connection between the first and second resistors being connected to the gate of a pfet device P0, and the gate-source voltage of the pfet P0 $Vgp = Vcc*Rgp1/(Rgp1+Rgp2+Rgp3)$ when Vin is at logic 1 and N0s is turned on.

12. The simultaneous bi-directional data bus of claim 11, wherein each current source provides the same amount of current I0, and the pfet device P0 and the values of Rgp1, Rgp2 and Rgp3 are chosen to meet the following requirements:
the drain to source current Ids of P0 is I0 when $Vgp1 = Vcc*Rgp1/(Rgp1+Rgp2+Rgp3)$, and $Vgp1 - Vthp$, the threshold voltage of P0, $< (Vcc-I0*Z0)/2$, so that P0 is at saturation region/mode when turned on.

13. The simultaneous bi-directional data bus of claim 12, wherein when a logic high is applied to one or more of the gates of N1, N2 ...Nk, the corresponding capacitors are selected, and when Vin is transiting from a logic low to a logic high, the resistor Rgp2 is shorted by the compensation capacitors.

14. A printed circuit board (PCB) communicating over a simultaneous bi-directional data bus having a characteristic impedance Z0, the PCB having a first driver unit and receiver unit connected to a first terminal end of the simultaneous bi-directional data bus, the driver unit having a sourcing current source and a first resistor connected in parallel between a voltage supply and the first terminal end of the simultaneous bi-directional data bus, and a sinking current source and a second resistor connected in parallel between a ground and the first terminal end of the simultaneous bi-directional data bus, wherein a substantially higher impedance of each current source relative to a substantially lower impedance of each resistor connected in parallel to the current source provides a relatively constant impedance in the first driver unit which substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

15. The PCB of claim 14, the PCB further including thereon:

the simultaneous bi-directional data bus;

a second driver unit and receiver unit connected to a second terminal end of the simultaneous bi-directional data bus;

the second driver unit having a sourcing current source and a first resistor connected in parallel between a voltage supply and a second terminal end of the simultaneous bi-directional data bus, and a sinking current source and a second resistor connected in parallel between a ground and the second terminal end of the simultaneous bi-directional data bus, wherein a substantially higher impedance of each current source relative to a substantially lower impedance of each resistor connected in parallel to the current source provides a relatively constant impedance in the second driver unit which substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

16. The PCB of claim 15, where in each of the first driver unit and the second driver unit, the first resistor of the sourcing current source and the second resistor of the sinking current source is substantially equal to twice the characteristic impedance of the simultaneous bi-directional data bus.

17. The PCB of claim 15, wherein the sourcing current sources of each of the first driver unit and the second driver unit are identical sourcing current sources, and the sinking current sources of each of the first driver unit and the second driver unit are identical sinking current sources.

18. The PCB of claim 15, wherein each driver unit comprises a p side driver and an n side driver which are serially connected between a voltage supply and ground, with the connection between the serially connected drivers being coupled to the simultaneous bi-directional data bus, and each driver unit having an output impedance of twice the characteristic impedance of the simultaneous bi-directional data bus so that the total

output impedance of each driver unit matches the characteristic impedance of the simultaneous bi-directional data bus.

19. The PCB of claim 15, wherein each driver unit includes a set of programmable compensation capacitors to compensate for parasitic capacitance and to accelerate transitions to higher speeds.

20. A method of transmitting simultaneous bi-directional data over a bus comprising:

providing a simultaneous bi-directional data bus having a characteristic impedance Z0;

connecting a first driver unit and receiver unit to a first terminal end of the simultaneous bi-directional data bus;

connecting a second driver unit and receiver unit to a second terminal end of the simultaneous bi-directional data bus;

substantially matching the characteristic impedance of each of the first driver unit and the second driver unit to the simultaneous bi-directional data bus by providing each of the first driver unit and the second driver unit with a sourcing current source and a first resistor connected in parallel between a voltage supply and a terminal end of the simultaneous bi-directional data bus, and a sinking current source and a second resistor connected in parallel between a ground and a terminal end of the simultaneous bi-directional data bus, wherein a substantially higher impedance of each current source relative to a substantially lower impedance of each resistor connected in parallel to the current source provides a relatively constant impedance in each driver unit which substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

21. The method of claim 20, including, providing in each of the first driver unit and the second driver unit the first resistor of the sourcing current source and the second resistor

of the sinking current source with an impedance equal to substantially twice the characteristic impedance of the simultaneous bi-directional data bus.

22. The method of claim 20, including providing the sourcing current sources of each of the first driver unit and the second driver unit as identical sourcing current sources and the sinking current sources of each of the first driver unit and the second driver unit as identical sinking current sources.

23. The method of claim 20, including providing each driver unit as a p side driver and an n side driver which are serially connected between a voltage supply and ground, coupling the connection between the serially connected drivers to the simultaneous bi-directional data bus, and providing each driver unit with an output impedance of substantially twice the characteristic impedance of the simultaneous bi-directional data bus so that the total output impedance of each driver unit substantially matches the characteristic impedance of the simultaneous bi-directional data bus.

24. The method of claim 20, including providing each driver unit with a set of programmable compensation capacitors to compensate for parasitic capacitance and to accelerate transitions to higher speeds.